2.5A 5V E-Fuse with Bi-Directional Protection Switch and DevSleep/Disable Mode

Description

The LX8233 is a fast acting bi-directional eFuse switch designed both to protect circuitry connected to its output (VOUT) from transient input voltage surges on its input (VCC), and to protect VCC from overload current events coming from the load on VOUT. It will also block the reverse discharge current from flowing from VOUT to VCC if the input supply collapes.

Voltage protection features include under-voltage lockout (UVLO), and over-voltage clamping. This clamp limits VOUT voltage allowing continued circuit operation during an input over-voltage transient condition, while UVLO ensures that VOUT remains off until VCC reaches its minimum operating threshold. On the current side, the LX8233 protects the input from a output short circuit and/or over current condtion with a 2.5A current limit circuit.

Another protection feature is latching thermal shutdown of VOUT, with a fault flag output on the combined EN/FAULT pin. Once thermal shutdown threshold is reached and the eFuse switch opens, the tristate EN/FAULT pin will be pulled to about 1.6V signaling to the system and potentially other connected eFuse switches that a fault has occurred. The LX8233 latches at this level until reset by the Enable pin, DEVSLP pin, or there is a VCC power recycle.

At device power up the user can initialize the DevSleep pin functionality and VOUT slew rate in one of two modes depending on the state of the FET_ON pin. In DevSleep Disabled Mode the slew rate is set to 13ms, and VOUT shutdown is engaged when the DEVSLP pin is toggled high regardless of the state of the FET_ON pin. In DevSleep Enabled Mode the slew rate is reduced to 1.4ms, and shutdown is engaged when the DEVSLP pin is toggled high and the FET_ON pin is low.

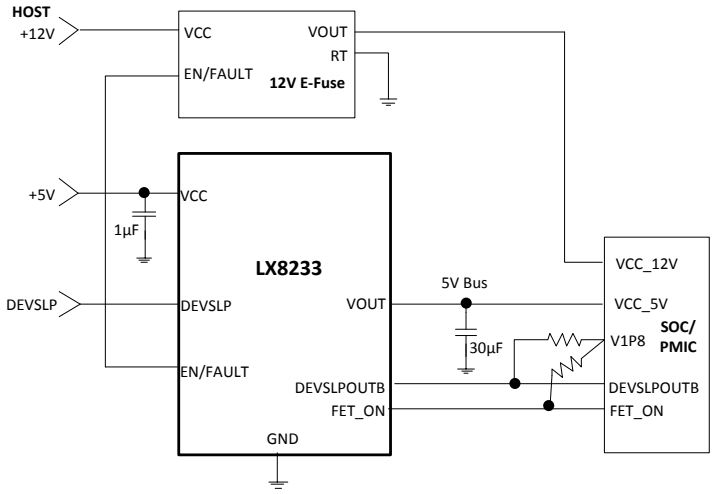
Features

- 50mΩ (typ.) Rdson Internal eFuse FET Protected From 15V
- Bi-directional Current Blocking Switch
- SATA DevSleep Support
- SAS-DISABLE Support
- Up to 15V Transient Input Range
- 6V Output Voltage Clamp
- Continuous Operation During VCC surge
- Current Limit at Overload and Short-Circuit Protection
- Over-Temperature Protection
- Selectable Soft-start 13ms or 1.4ms Risetime
- UVLO Detection
- VQFN 2mm x 3mm 13L Package

Applications

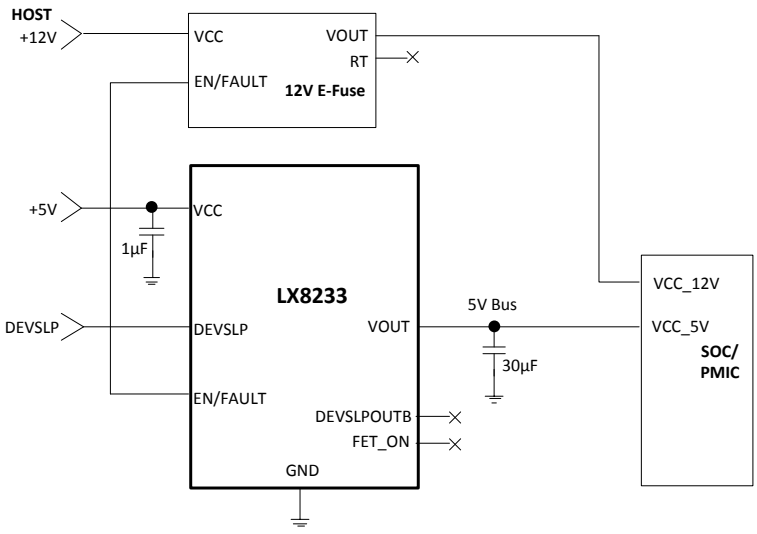
- Hard-Disk Drive
- Solid-State Drive
- Hot Swap
- PC Cards

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DevSleep Enabled Mode

Figure 1 · **Typical Application of LX8233, DevSleep Enable Mode**



DevSleep Disabled Mode

Figure 2 · **Typical Application of LX8233, DevSleep Disable Mode**

Pin Configuration and Pinout

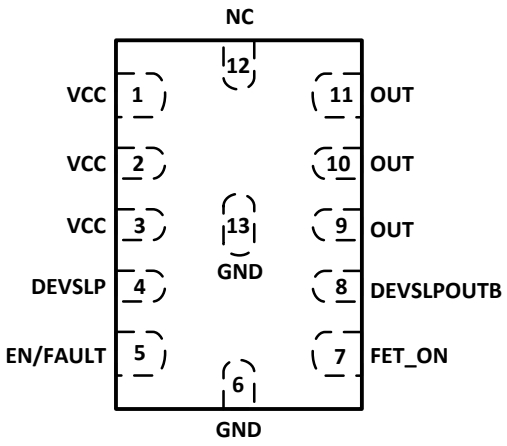


Figure 3 · **Pinout VQFN 2mm x 3mm 13L Top View**

Marking: Line 1 MSC
Line 2 8233
Line 3 Date / Lot Code

Ordering Information

Ambient Temperature	Type	Package	Part Number	Packaging Type
-40°C to 85°C	RoHS Compliant, Pb-free	VQFN 2mm x 3mm 13L	LX8233ILQ	Bulk / Tube
			LX8233ILQ-TR	Tape and Reel

Pin Description

<table>
<tr><th>Pin Number</th><th>Pin Designator</th><th>Input/ Output</th><th>Description</th></tr>
<tr><td>1, 2, 3</td><td>VCC</td><td>Input</td><td>Input of the device.</td></tr>
<tr><td>4</td><td>DEVSLP</td><td>Input</td><td>DevSleep mode input. There are two modes for the usage of DEVSLP.
One operational mode is DEVSLP Enable Mode. It is selected by connecting the FET_ON pin of LX8233 to SOC during power on initalization. In this mode, only when FET_ON is low will setting DEVSLP high shut down the LX8233. This handshake feature allows the SOC to override the shutdown process initiated by the host using DevSleep allowing any necessary housekeeping functions to complete before powering off the switch. When in this mode the VOUT softstart time is programmed to 1.4 ms.
The other mode is DEVSLP Disabled Mode. This is selected by letting FET_ON pin float during power on initalization. In this mode the LX8233 will shutdown by setting DEVSLP high regardless of the FET_ON state. When in this mode the VOUT softstart time is programmed to 13 ms.
The two mode are summarized in the table below.
<table>
<tr><th></th><th>DEVSLP Disabled</th><th>DEVSLP Enabled</th></tr>
<tr><td>FET_ON</td><td>Float</td><td>Connected to SOC</td></tr>
<tr><td>T_{RISE}</td><td>~13ms</td><td>~1.4ms</td></tr>
<tr><td>Shutdown</td><td>DEVSLP High</td><td>(DEVSLP High) AND (FET_ON Low)</td></tr>
</table></td></tr>
<tr><td>5</td><td>EN/FAULT</td><td>Input/Output</td><td>The EN/FAULT pin is a tri−state, bidirectional interface. It can be used to disable the output of the device by pulling it to ground using an open drain or open collector device. If a thermal fault occurs, the voltage on this pin will go to an intermediate state (~1.6V)to signal a monitoring circuit that the device is in thermal shutdown. It can also be connected to another device in this family to cause a simultaneous shutdown during thermal events. See simplified schematic in Theory of Operation/ Application section.</td></tr>
<tr><td>6</td><td>GND</td><td>-</td><td>Ground Pin (Pin 6 and Pin 13 are internally connected).</td></tr>
<tr><td>7</td><td>FET_ON</td><td>Input</td><td>DEVSLP mode is configured by the FET_ON state during power on initializaiton.
When FET_ON is floating (50pf maximum pin capacitance), the LX8233 is set to DEVSLP Disabled Mode. In this mode, the LX8233 can be shut down by setting the DEVSLP pin high.
When FET_ON is connected to SOC, the LX8233 can only be shut down by setting both DEVSLP high and FET_ON low.</td></tr>
<tr><td>8</td><td>DEVSLPOUTB</td><td>Output</td><td>Open-drain output. A pull-up resistor is connected to the I/O supply of SOC. DEVSLPOUTB is the inversed polarity version of DEVSLP.</td></tr>
<tr><td>9, 10, 11</td><td>VOUT</td><td>Output</td><td>Output of the device, connect to circuitry to be protected. A 10uF capacitor is needed for over voltage protection stability. The capacitor return should be connected directly to the GND pin.</td></tr>
<tr><td>12</td><td>NC</td><td>-</td><td>Do Not Connect.</td></tr>
<tr><td>13</td><td>GND</td><td>-</td><td>Ground Pin(Pin 6 and Pin 13 are internally connected).</td></tr>
</table>

Block Diagram

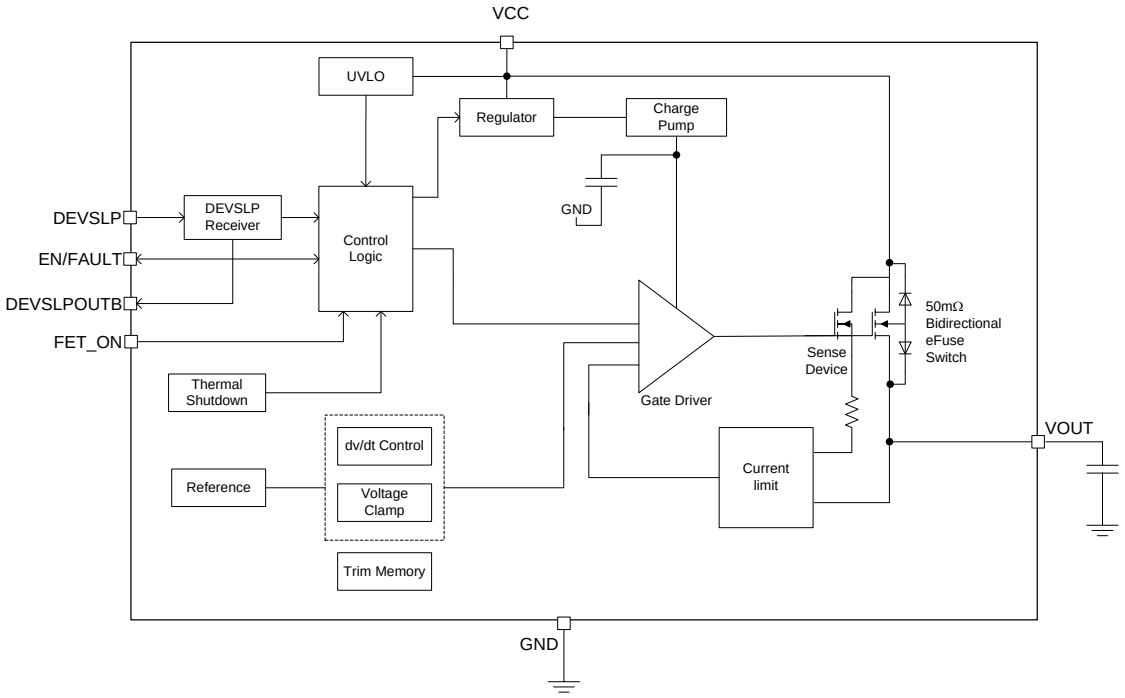


Figure 4 · **Simplified Block Diagram of LX8233**

Absolute Maximum Ratings

Parameter	Min	Max	Units
VCC to GND (Steady-State)	-0.3	15	V
VCC to GND (Transient 100ms)	-0.3	15	V
VOUT to GND (Steady-State)	-0.3	6.5	V
VOUT to GND (Transient 100ms)	-0.3	7	V
EN/FAULT to GND	-0.3	≤VCC	V
EN/FAULT to GND	-0.3	6	V
DEVSLPOUTB to GND	-0.3	6	V
DEVSLP to GND	-0.3	3.6	V
FET_ON to GND	-0.3	3.6	V
ESD (Human Body Model)	2000		V
ESD (Charged Device Model)	1000		V
Power Dissipation		1.3	W
Storage Temperature	-65	150	°C

Note: Performance is not necessarily guaranteed over this entire range. These are maximum stress ratings only. Exceeding these ratings, even momentarily, can cause immediate damage, or negatively impact long-term operating reliability

Operating Ratings

	Min	Max	Units
VCC	4.2	5.75	V
I(VCC)		2.5	A
Junction Temperature	-40	125	°C

Note: Performance is generally guaranteed over this range as further detailed below under Electrical Characteristics.

Thermal Properties

Thermal Resistance	Typ	Units
θ_{JA}	40	°C/W

Note: The θ_{JA} numbers assume no forced airflow. Junction Temperature is calculated using $T_J = T_A + (PD \times \theta_{JA})$. In particular, θ_{JA} is a function of the PCB construction. The stated number above is for a four-layer board in accordance with JESD-51 (JEDEC).

Electrical Characteristics

Note: The following specifications apply over the operating ambient temperature of -40°C ≤ T_A ≤ 85°C except where otherwise noted with the following test conditions: VCC = 5V. Typical parameter refers to T_J = 25°C.

Symbol	Parameters	Test Conditions/Comments	Min	Typ	Max	Units
eFuse FET						
T_{ONDLY}	Turn-on Delay Time	Enable by EN/FAULT with load current 100mA.		80		µs
R_{DSON}	On Resistance	T_A = 25°C, (Note 2)		50		mΩ
		T_J = 80°C, (Note 1)		95		mΩ
I_{OFF}	Off State Output Leakage Current	VCC = 12V_{DC}, EN/FAULT = GND, VOUT = GND Measure I(VOUT)			1	µA
I_{DC}	Continuous Current	T_A = 25°C		2		A
T_{RISE}	VOUT Rise Time	FET_ON = Float	10.4	13	15.6	ms
		FET_ON = GND		1.4		ms
Thermal Shutdown						
T_{SD}	Shutdown Temperature	OUT is latched off once thermal shutdown is triggered. It can be reset three ways. 1) EN/FAULT is pulled low then let float. 2) DEVSLP pin is toggled high then low. 3) VCC is recycled.		135		°C
Under/Over Voltage Protection						
V_{CLAMP}	Output Clamping Voltage	VCC = 10V	5.75		6.25	V
	Maximum Overshoot During Transient	VCC transient from 5V to the higher than 12V at 100V/µs with I_{VOUT} = 0A. C_{OUT}=33uF			6.5	V
	Minimum Undershoot During Transient	VCC transient from 5V to the higher than 12V at 100V/µs with I(VOUT) = 2.5A. C_{OUT}=33uF	4.5			V
V_{UVLO_TH}	Under-Voltage Lock-Out Threshold	Turn-on and voltage increases	3.75		4.2	V
V_{UVLO_HYS}	Under-Voltage Lock-Out Hysteresis			0.3		V
	Under-Voltage Lock-Out Response Time			2		µs
Current Protection						
I_{SC_LIM}	Short Circuit Current Limit	VOUT is <1V from GND.		2.5		A
I_{AVG_LIM}	Overloading Current Limit	VOUT is 0.5V lower than the nominal VOUT.	2.5	3		A

Symbol	Parameters	Test Conditions/Comments	Min	Typ	Max	Units
Reverse Current Detection						
Ireverse	Reverse Current Limit		0.9	1.32	2.1	A
treverse	Reverse Current Limit Response Time	VCC DV/DT = -5V/1ms		2		µs
DEVSLP						
$DEVSLP_{TH}$	Logic Input Threshold	Measure the threshold	0.8		2.0	V
$DEVSLP_{HYS}$	Logic Input Hysteresis	Measure the threshold of DEVSLP		190		mV
$DEVSLP_{MAX}$	Maximum DEVSLP Pin Voltage	Design target. No test.			3.3	V
DEVSLP-ΩIN	Input Impedance	Output Enabled, Unconnected pin = Enabled. Internal pull-down resistor test. Measure the impedance from DEVSLP to GND	350	500	1000	kΩ
DEVSLP-OFF-TDLY	Turn-off Deglitch Delay	100mA VOUT load. Logic Turn off by changing DEVSLP from 0V to 5V. Measure the delay from the edge of DEVSLP to 4.5V(the 10% lower to 5V VOUT).	2		50	µs
DEVSLP-ON-TDLY	Turn-on Deglitch Delay	100mA VOUT load. Logic Turn on by changing DEVSLP from 5V to 0V. Measure the delay from the edge of DEVSLP to 0.5V(the 10% of 5V VOUT).	2		300	µs
EN/FAULT						
VEN_{DISIL}	Disable Logic Input Level Low	Output disabled			0.4	V
VEN_{MIDIL}	Thermal Fault Input Logic Level Low	EN/FAULT pin is driven by the other eFuse. Thermal Fault, Output Disabled,			1.0	V
VEN_{MIDIH}	Thermal Fault Input Logic Level Low	EN/FAULT pin is driven by the other eFuse. Thermal Fault, Output Disabled,	2.1			V
VEN_{ENIH}	Enable Logic Input Level High	Output Enabled	3.3			V
	High State Max Voltage	(Note 1)			5.2	V
VEN_{MIDOL}	Thermal Fault Output Logic Level Low	LX8233 drives EN/FAULT pin. Thermal Fault, Output Disabled,	1.1			V
VEN_{MIDOH}	Thermal Fault Output Logic Level Low	LX8233 drives EN/FAULT pin. Thermal Fault, Output Disabled,			1.9	V
$IIL_{EN/FAULT}$	Logic Low Input Sink Current	V_{EN} = GND at the normal operation		10		µA
		V_{EN} = GND at the thermal shutdown		20		µA

Symbol	Parameters	Test Conditions/Comments	Min	Typ	Max	Units
$IIH_{EN/FAULT}$	Logic High Leakage Current	V_{EN} = 4.3V			1	µA
DEVSLPOUTB						
V_{PGPD}	Pull-down Voltage	I_{SINK} = 4mA, sinking current into DEVSLPOUTB			0.3	V
I_{PGLEAK}	Leakage Current	$V_{DEVSLPOUTB}$ = 1.8V			1	µA
FET_ON (Note 3)						
	Logic threshold low-to-mid		0.3	0.5	0.7	V
	Logic threshold mid-to-high		0.8	1.0	1.2	V
	Input leakage current	FET_ON = GND			1	µA
Total Device						
I_{Q_OP}	Bias Current	Operational		165	250	µA
I_{Q_DIS}		Disable (EN/FAULT = GND or DEVSLP = High)		104		µA
I_{Q_FLT}		Thermal Fault Latch Off		100		µA
V_{MIN}	Minimum Operating Voltage	(Note 4)			4.2	V
	Reverse Bias Leakage Current	VCC = GND, VOUT = 5V		4		µA

Note: 1. Guaranteed by Design

Note: 2. Pulse test: Pulse width = 300µs, Duty cycle = 2%.

Note: 3. Total pin capacitance must be ≤50pf to be considered floating by the chip.

Note: 4. Device may shut down prior to reaching this level based on actual UVLO trip point.

Theory of Operation / Application Information

DevSleep Logic Operation

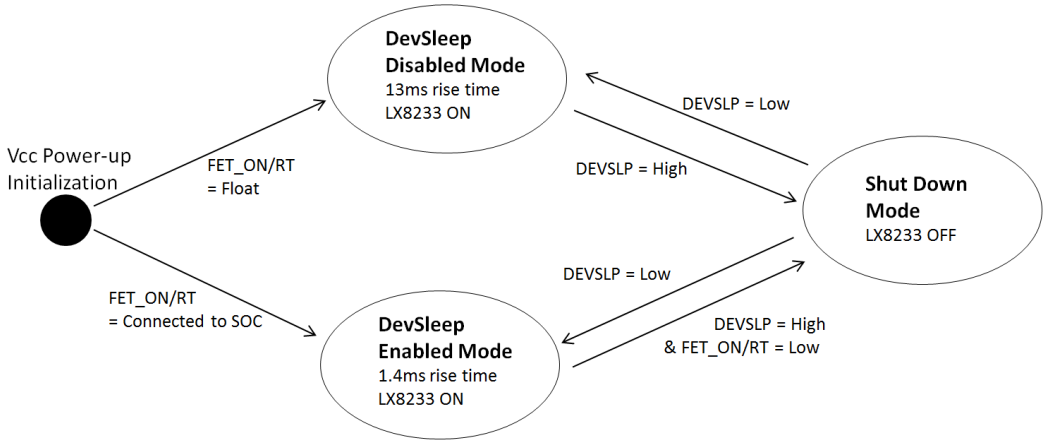


Figure 5 · **DevSleep Operation**

VCC Power-up Initialzation: As VCC rises the LX8233 initializes its internal circuits. Upon reaching the UVLO threshold the LX8233 also detects the status of FET_ON pin. If FET_ON detectes a float condition it initializes in DevSleep Disabled Mode. However if FET_ON is detected as connected to SOC then it initalizes to DevSleep Enabled Mode.

DevSleep Disabled Mode: When VCC reaches the UVLO threshold, VOUT slews for 13ms from 0V to VCC. The LX8233 is monitoring the DEVSLP pin and enters Shutdown Mode. if DEVSLP goes high.

DevSleep Enabled Mode: When VCC reaches the UVLO threshold, VOUT slews for 1.4ms from 0V to VCC. In this mode, the LX8233 is monitoring both the DEVSLP and FET_ON pins. When both DEVSLP goes high and FET_ON goes low, LX8233 enters Shutdown Mode.

Shut Down Mode: Once LX8233 enters this mode the chip shuts down VOUT and most internal circuitry minimizing quiescent current to that required to monitor the DEVSLP pin and maintain state information. When DEVSLP toggles low, the LX8233 restores itself to original DevSleep Disabled/Enabled Mode operation mode.

EN/FAULT Operation

EN/FAULT is typically floated and connected as common node between the parallel connected devices. There is an a weak (~430kΩ) internal pull-up resistor, so the EN/FAULT pin goes to ~4.3V when VCC = 5V. However when parallel connected the actual voltage depends on the mismatch between the internal regulator supply voltages. To disable VOUT using the EN/FAULT pin you must use an external pull-down device, however the internal pull-up resistor will enable VOUT without any external signal.

If the IC's junction temperature passes the thermal shutdown threshold the LX8233 will pull down the EN/FAULTpin to the mid-level fault logic condition. As shown in the simplified schematic below an internal switch (thermal latch) engages at thermal shutdown driving the EN/FAULT pin to approximately 1.6V with pulldown capability to drive several parallel connected devices. Thus if LX8233 reaches thermal shutdown it will latch off all the parallel connected devices on the same

node. It remains at 1.6V until either the Enable Pin is pulled low then left to float, the DEVSLP pin is toggled (high then low, or low to high), or there is a VCC power recycle.

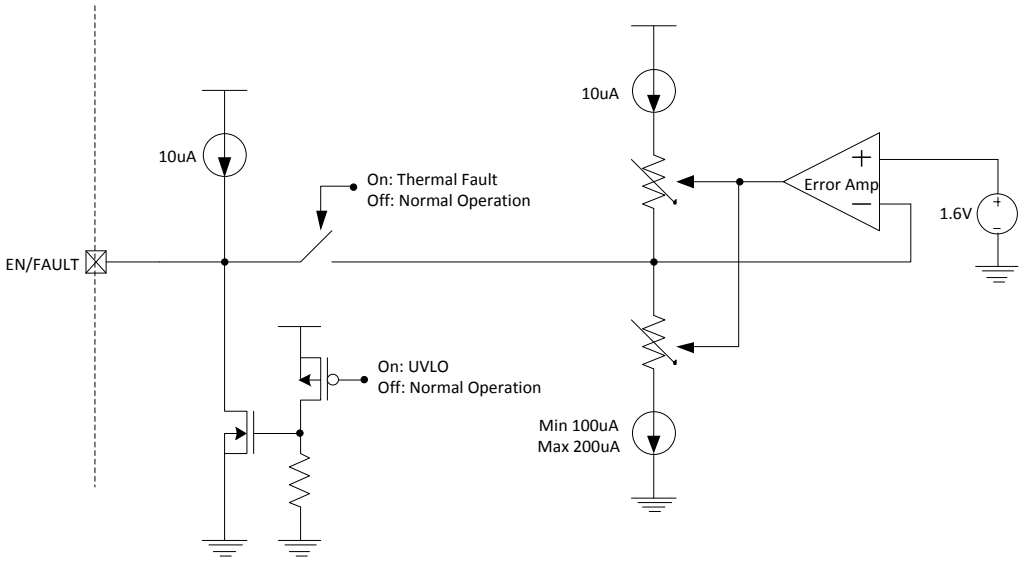
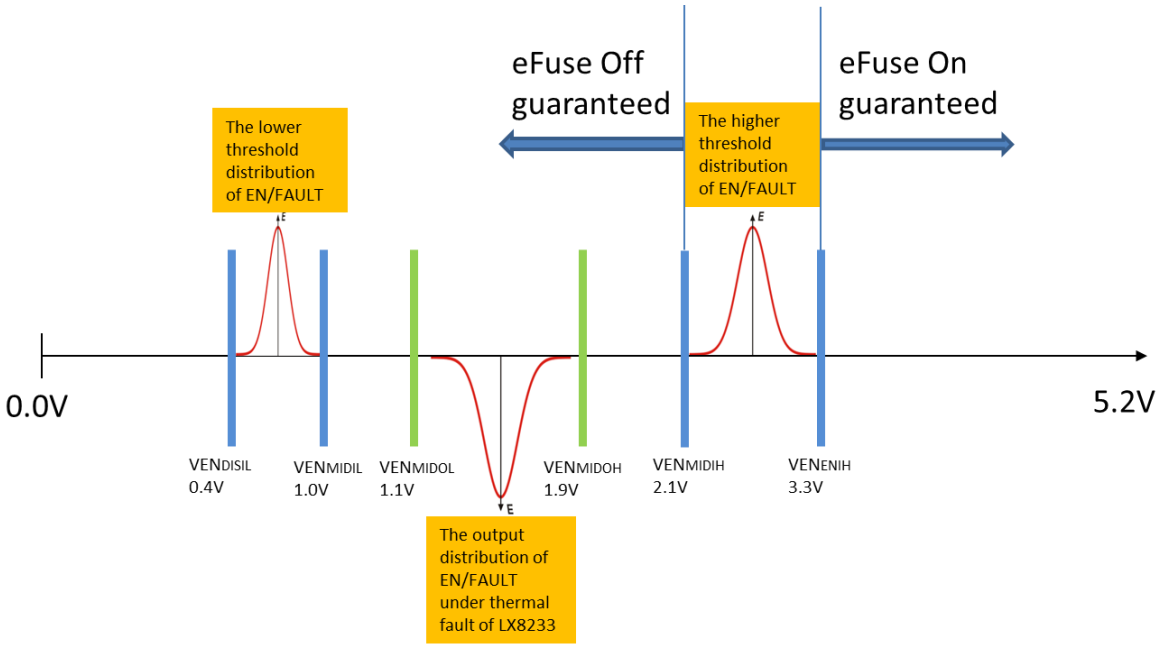


Figure 6 · **Simplified EN/FAULT circuitry**

IReverse	UVLO	DEVSLP	THERM	ENABLE
0	0	0	0	1
0	0	0	1	mid
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

EN/FAULT node is share with a secondary eFuse in order to shutdown the secondary eFuse for the case SAS-Disable or DevSleep mode, thermal fault and UVLO condition. It will gurantee the secondary eFuse never turns on when LX8233 is under the specific condition like SAS-Disable, DevSleep, thermal fault and UVLO conditions. The EN/FAULT responses are listed in the following table.

	eFuse	**EN/FAULT as OUTPUT**	**Effect on the secondary part**
UVLO	eFuse is turned off.	Ground. Drive EN/FAULT is lower than 0.4V	Disable the secondary part.



Thermal Fault	eFuse is turned off. The thermal shutdown is latched off. It can be reset by VIN recycle, DEVSLP toggle or EN/FAULT toggle.	Mid point. Drive EN/FAULT lower than 1.9V higher than 1.1V	Disable the secondary part.
DEVSLP (SAS-DISABLE)	eFuse is turned off.	Ground. Drive EN/FAULT is lower than 0.4V	Disable the secondary part.

Reverse Current Protection

While the simplest protection against a reverse current condition maybe a diode in series connection to the load, this method has drawbacks. There is significant power loss in the forward conduction mode, as well as poor supply rail regulation. In order to solve this problem, the LX8233 implements a bidirectional voltage and current blocking FET switch. The basic concept of this method is to detect the polarity of voltage drop through the FET pass device and open up the switch to block reverse current. This method is very effective for fast slew rate of reverse current blocking. If the slew rate of the reverse current is slower than a certain rate (i.e. a slowly reducing input voltage), the reveser current will be allowed until the input voltage reaches the UVLO threshold. Below this level, the switch is quickly turned off and blocks reverse current and voltage.

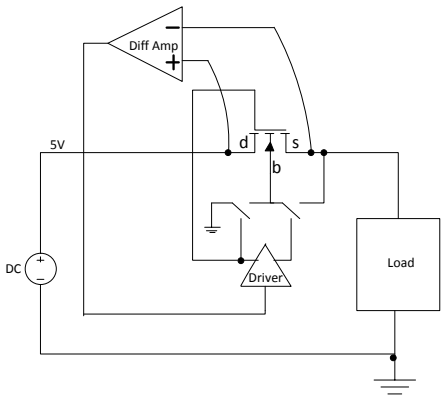


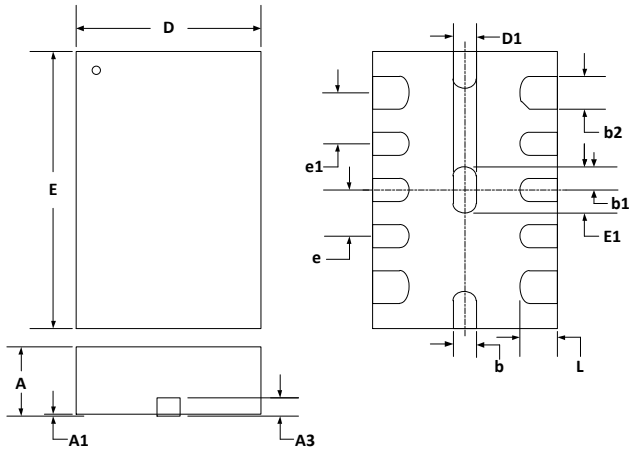
Figure 7 · **Simplified reverse current dectection circuitry**

Under-Voltage Lock-Out

In LX8233, UVLO plays an important role. It has a high threshold with very little hystresis and a very fast comparator propagation delay. These features of UVLO circuit maximize the reverse current blocking function capability.

UVLO	EN/FAULT	DEVSLP	FET_ON	LX8233	DEVSLPOUTB with pullup
violated	*	*	*	off	off/high

Package Outline Dimensions



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A		1.00		0.039
A1	0.00	0.05	0.000	0.002
A3	0.203 REF		0.008REF	
D	1.95	2.05	0.077	0.081
b	0.20	0.30	0.008	0.012
D1	0.20	0.30	0.008	0.012
L	0.35	0.45	0.014	0.018
E	2.95	3.05	0.116	0.120
e	0.50BSC		0.020BSC	
e1	0.575BSC		0.023BSC	
b1	0.18REF		0.007REF	
b2	0.35	0.45	0.014	0.018
E1	0.38	0.48	0.015	0.019

Figure 8 · **LQ 12-Pin VQFN Package Dimensions**

Note: 1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm (.006”) on any side. Lead dimension shall not include solder coverage.

Note: 2. Dimensions are in mm, inches are for reference only.

Land Pattern Recommendation

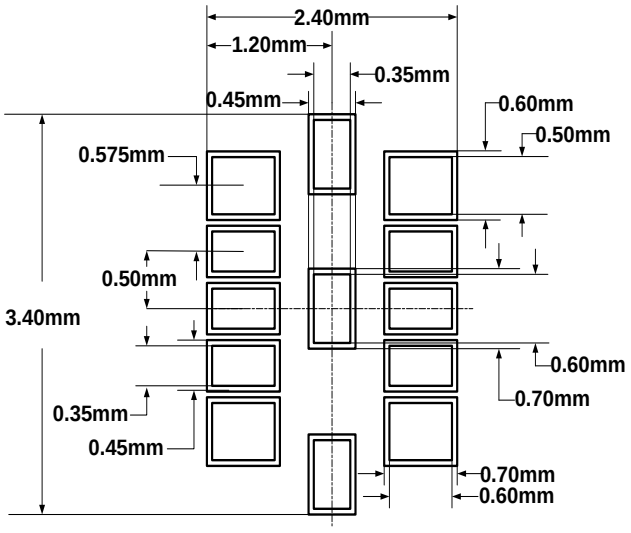


Figure 9 · **LQ 12-Pin VQFN Package Land Pattern**

Disclaimer:
This PCB land pattern recommendation is based on information available to Microsemi by its suppliers. The actual land pattern to be used could be different depending on the materials and processes used in the PCB assembly, end user must account for this in their final layout. Microsemi makes no warranty or representation of performance based on this recommended land pattern
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Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA

Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

E-mail: sales.support@microsemi.com

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